What is claimed is:

1. A cell searching apparatus which searches for a cell based on a received asynchronous wideband direct-sequence code division multiple access (DS/CDMA) signal in a receiver, the received signal including a data channel and a synchronous channel composed of a primary synchronization code commonly used in every cell and a secondary synchronization code indicating a code group unique to each cell, the cell searching apparatus comprising:

a code group identifying unit for estimating and compensating for a frequency error between the synchronous channel and an internally generated primary synchronization code, estimating and compensating for channel characteristics which the synchronous channel has experienced, and correlating the compensated synchronous channel with available secondary synchronization codes, thereby identifying the code group; and

a scrambling code identifying unit for correlating a plurality of scrambling codes belonging to the code group with the data channel, thereby obtaining a scrambling code unique to each cell.

2. The cell searching apparatus of claim 1, wherein the code group identifying unit comprises:

a primary synchronization code generator,

a frequency error compensator for estimating a frequency error between the synchronous channel and a primary synchronization code generated by the primary synchronization code generator and compensating the synchronous channel for the estimated frequency error;

a channel compensator for estimating channel characteristics from the frequency error compensated synchronous channel and compensating the frequency error compensated synchronous channel for the estimated channel characteristics; and

a code group identifier for combining the results of correlating the channel characteristics compensated synchronous channel with the available plurality of primary synchronization codes, thereby identifying the code group.

3. The cell searching apparatus of claim 2, wherein the frequency error compensator comprises:

a switch having an input and a first and a second output and operating such that the synchronous channel can be received through the input;

a frequency error estimator connected to the first output of the switch, the frequency error estimator obtaining the phase difference between the synchronous

channel and the primary synchronization code generated by the primary synchronization code generator and converting the phase difference into a frequency error;

a numerically controlled oscillator for generating a complex sinusoidal wave corresponding to the frequency error; and

a multiplier connected to the second output of the switch, the multiplier multiplying the synchronous channel input through the switch by the complex sinusoidal wave.

4. The cell searching apparatus of claim 3, wherein the frequency error estimator comprises:

a plurality of partial correlation units each for correlating the synchronous channel divided into a predetermined number of blocks in each slot with the primary synchronization code generated by the primary synchronization code generator;

a divider for dividing one output by another output among the outputs of the partial correlation units, the two outputs being separated from each other by a predetermined chip duration;

a phase arithmetic unit for obtaining a phase from the outputs of the divider; and

a multiplier for converting the phase into a frequency by dividing the output of the phase arithmetic unit by the predetermined period of time.

5. The cell searching apparatus of claim 4, wherein the frequency error estimator further comprises an averager for summing up the output of the divider a predetermined number of times and averaging the sum of the outputs using the predetermined number of times.

6. The cell searching apparatus of claim 2, wherein the code group identifier comprises:

a plurality of correlation units for correlating the output of the channel compensator with the plurality of secondary synchronization codes;

a coherent combiner for summing up the outputs of the correlation units and squaring the sum of the outputs; and

a selection means for selecting a secondary synchronization code at which the output of the coherent combiner exceeds a predetermined value.

7. A method of acquiring a scrambling code included in a code group from an asynchronous wideband direct-sequence code division multiple access

(DS/CDMA) signal received in an asynchronous wideband DS/CDMA receiver, the received signal including a data channel and a synchronous channel composed of a primary synchronization code commonly used in every cell and a secondary synchronization code indicating a unique code group of each cell, the scrambling code being a spreading code unique to each cell, the method comprising:

(a) estimating and compensating for a frequency error between the synchronous channel and a primary synchronization code generated by a primary synchronization code generator;

(b) estimating and compensating for characteristics of a channel which the synchronous channel has experienced;

(c) correlating the compensated synchronous channel with available secondary synchronization codes, thereby identifying a secondary synchronization code included in the synchronous channel; and

(d) correlating a plurality of scrambling codes belonging to a code group represented by the secondary synchronization code with the data channel to obtain a scrambling code unique to each cell.

8. The method of claim 7, wherein (a) further comprises:

(a1) dividing the synchronous channel into a predetermined number of blocks in each slot and correlating the divided synchronous channel with the primary synchronization code generated by the primary synchronization code generator;

(a2) dividing one output by the other output among the results of the correlation, the two results of the correlation being separated from each other by a predetermined chip duration;

(a3) obtaining a phase from the result of the division;

(a4) dividing the phase by the predetermined period of time to convert the phase into a frequency; and

(a5) compensating the synchronous channel for the frequency.

9. The method of claim 8, wherein in (a1), each of the blocks of the synchronous channel has a chip length which is integral times of 16.

10. The method of claim 8, wherein in (a2), the predetermined period of time corresponds to 1/2 of a chip length of the synchronous channel.